UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,347	07/02/2003	Varadarajan Srinivasan	NLMI.P210	5158

25670 7590 05/18/2007

WILLIAM L. PARADICE, III
4880 STEVENS CREEK BOULEVARD
SUITE 201
SAN JOSE, CA 95129

EXAMINER	
WU, JIANYE	
ART UNIT	**PAPER NUMBER**
2609	

MAIL DATE	DELIVERY MODE
05/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/613,347	SRINIVASAN ET AL.	
	Examiner	Art Unit	
	Jianye Wu	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/02/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1-3, 5-9, 12, 16-36** are rejected under 35 U.S.C. 102(b) as being anticipated by Ohgane et al, US Patent Number 5,875,173, herein after being referenced as Ohgane et al.

Regarding **claim 1**, Ohgane et al discloses a traffic management processor (FIG.1) for processing an UBR (ABR, line 5, Col 5 in specification) traffic flow and a CBR (line 5, Col 5 in specification) traffic flow, comprising:

a departure DTC circuit (34 of FIG. 2) for calculating a departure (Line 22-24, Col. 7);

a CAM device coupled to the DTC circuit and having a plurality of rows (511 and 512 of FIG. 4), each row including a first portion for storing the departure time ("Transmission Time" in 511 of FIG. 4) for a corresponding packet and including a second portion for storing a CBR bit (513 of FIG. 4) indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow; and

compare logic (516 of FIG 4, or a combination of 40 and 51 of FIG. 3) coupled to the CAM device and configured to determine which of the departure times stored in the CAM device is the earliest (FIG. 5, the packet with the earliest departure time is sent).

Regarding **claim 2**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above), wherein the packets of the CBR traffic flow and packets of the UBR traffic flow are queued in the same queuing mechanism (511 and 513 of FIG. 4).

Regarding **claim 3**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above); wherein an asserted CBR bit indicates the departure time corresponds to a packet of the CBR traffic flow, and a de-asserted CBR bit indicates the departure time corresponds to a packet of the UBR traffic flow (511 and 513 of FIG. 4).

Regarding **claim 5**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above), wherein departure times ("Transmission Time" in 511 of FIG. 4) comprise counter values generated by a counter circuit (50 in FIG. 4) in response to state transitions of a clock signal.

Regarding **claim 6**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above), wherein the departure times can be stored in the CAM device (51 of FIG. 4) in any order (511 of FIG. 4), regardless of priority.

Regarding **claim 7**, Ohgane et al discloses the traffic management processor of Claim 1, further comprising a priority encoder (514 of FIG. 4).

Regarding **claim 8**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above), further comprising:

a match line (the line from 516 to 511 of FIG. 4) coupled to each row of the CAM device;

a word line (the lines from 512 to 511 of FIG. 4) coupled to each row of the CAM device; and

means for selectively driving (paragraph 4-6 of Col. 8) each word line in response to match condition indicated on the corresponding match line.

Regarding **claim 9**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above), wherein compare logic is configured to compare the departure times (S9-S11 of FIG. 5) by the CAM device (51 of FIG. 4) with each other to determine which departure time is the earliest (S9-S12 of FIG. 5).

claim 10, Ohgane et al discloses the traffic management processor of Claim 9 (as applied in claim 9 above), wherein the CAM device selectively provides the departure times to the compare logic in response to the CBR bits (Line 20-25 of Col. 6, where different traffic parameters are used to calculate departure times of packets depend on their CBR bits).

Regarding **claim 12**, Ohgane et al discloses the traffic management processor of Claim 1 (as applied in claim 1 above), wherein the CAM device (51, FIG. 3) further includes an input (the input to 51 from 50 in FIG. 3) to receive a current time value.

Regarding **Claim 16**, Ohgane et al discloses a traffic management processor (FIG. 1) for processing a plurality of packets each having a control bit indicating whether the packet belongs to a traffic flow UBR or belongs to a traffic flow CBR, comprising:

means for generating (Line 22-30, Col. 7) a departure time for each packet in response to the control bit (CBR mode and ABR mode, Line 20-24, Col. 6) contained within the packet;

means for queuing (511 and 513 of FIG. 4) the CBR packets and the UBR packets together in the same queue according to their departure times (511 of FIG. 4); and

means for selecting (516 of FIG. 4) the CBR packets and the UBR packets for transmission according to their departure times (FIG. 5).

Regarding **claim 17**, Ohgane et al discloses the traffic management processor of Claim 16 (as applied in claim 16 above), wherein the means for generating comprises:

a departure time calculator (Line 22-30, Col. 7) configured to calculate the departure times for CBR packets using a first expression (Line 20-22, 3rd paragraph of Col. 6, using the peak rates for UBR) and to calculate the departure times for UBR packets using a second expression (Line 22-24, 3rd paragraph of Col. 6, using the peak rates for ABR, which are different from those of CBR).

Regarding **claim 18**, Ohgane et al disclose the traffic management processor of Claim 16 (as applied in claim 16 above), wherein the means for queuing comprises:

a CAM device (51 of FIG. 4) having a plurality of rows (511 and 513 of FIG. 4), each row including a first portion for storing the departure time ("Transmission Time", 511 of FIG. 4) for a corresponding packet and including a second portion for storing the control bit (513 of FIG. 4).

Regarding **claim 19**, Ohgane et al discloses the traffic management processor of Claim 18 (as applied in claim 18 above), wherein the CAM device (51 of FIG. 3) includes an input (the input to 51 from 50 in FIG. 3) to receive a current time value and is configured to compare the current time value with CBR packets (FIG. 5, departure

times of all packets, including the CBR packets, are compared with a current time value).

Regarding **claim 20**, Ohgane et al discloses the traffic management processor of Claim 18 (as applied in claim 18 above), wherein the means for selecting comprises:

compare logic (a combination of 40 and 51 in FIG. 3) coupled to the CAM device (51 of FIG. 3) and configured to determine which of the departure times for the UBR packets and for the re-classified CBR packets is the earliest (FIG. 5, departure times of all packets, including the re-classified CBR packets, are compared with a current time value).

Regarding **claim 21**, Ohgane et al discloses the traffic management processor of Claim 20 (as applied in claim 20 above), wherein the compare logic (a combination of 40 and 51 in FIG. 3) compares the departure times with each other to determine which of the departure times is the earliest (S13, FIG. 5).

Regarding **claim 22**, Ohgane et al discloses a traffic management processor for simultaneously processing an UBR traffic flow and a CBR traffic flow, comprising:

a DTC circuit (34 of FIG. 2) configured to calculate (line 22-30, Col. 7) a departure time (transmission time, line 26, Col. 7) for each UBR packet and a departure time window (transmission time, line 26, Col. 7) for each CBR packet;

a queuing mechanism (511 and 513 of FIG. 4) coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together; and

compare logic (516 of FIG. 4, or a combination of 40 and 51 in FIG. 3) coupled to the queuing mechanism (511 and 513 of FIG. 4) and configured to select the packets for departure (FIG. 5).

Regarding **claim 23**, Ohgane et al discloses the traffic management processor of Claim 22 (as applied in claim 22 above), wherein queuing mechanism (516 of FIG. 4, combined with 40 in FIG. 3) is configured to always enable the UBR packets for departure and configured to selectively enable the CBR packets for departure (516 of FIG. 4).

Regarding **claim 24**, Ohgane et al discloses the traffic management processor of Claim 23 (as applied in claim 23 above), wherein the queuing mechanism enables each CBR packet for departure (511, 513 and 516, FIG. 4) when the CBR packet's departure time window comprises a current time value (S9, FIG. 5).

Regarding **claim 25**, Ohgane et al discloses the traffic management processor of Claim 24 (as applied in claim 24 above), wherein the queuing mechanism (511 and 513, FIG. 4) comprises a CAM device (511 and 513, FIG. 4).

Regarding **claim 26**, Ohgane et al discloses the traffic management processor of Claim 25 (as applied in claim 25 above), wherein the CAM device comprises:

a plurality of rows (511 and 513 of FIG. 4) each row having a first portion for storing the departure time (511 of FIG. 4) for a corresponding packet and having a second portion for storing a control bit (513 of FIG. 4) indicating whether the corresponding packet is part of the UBR traffic flow or is part of the CBR traffic flow; and

an input (the input to 511 from 50 via 516) to receive the current time value.

Regarding **claim 27**, Ohgane et al discloses the traffic management processor of Claim 22 (as applied in claim 22 above), wherein compare logic (516 of FIG. 4, or a combination of 40 and 51 in FIG. 3) compares the departure times with each other (S9-S11 of FIG. 5) to determine which of the departure times is the earliest (S9-S12 of FIG. 5).

Regarding **claim 28**, Ohgane et al discloses a method of processing a first traffic flow having an UBR and a second traffic flow having a CBR, comprising:

calculating a departure time (Line 22-24 of Col. 7) for each packet received;

storing the departure times (3rd paragraph of Col. 8) for packets belonging to all traffic flows in the same table, each departure time having a CBR bit (513 of FIG. 4);

asserting the CBR bit for each packet that belongs to the CBR traffic flow (513 of FIG. 4);

de-asserting the CBR bit for each packet that belongs to UBR traffic flow (513 of FIG. 4);

determining which of the departure times that have a de-asserted CBR bit is the earliest (511-516 in FIG. 4); and

transmitting the packet corresponding to the earliest departure time (FIG 5).

Regarding **claim 29**, Ohgane et al discloses the method of Claim 28 (as applied in claim 28 above), wherein the departure times having de-asserted CBR bits are compared (FIG. 5, all the departure times are compared, including the departure times having de-asserted CBR bits) with each other to which departure time is the earliest.

Regarding **claim 30**, Ohgane et al discloses the method of Claim 28 (as applied in claim 28 above), wherein the table (511 of FIG. 4) comprises a content addressable memory (511 of FIG. 4).

Regarding **claim 31**, Ohgane et al discloses the method of Claim 28 (as applied in claim 28 above), further comprising:

comparing (S9 of FIG. 5) a current time value (COUTNER in S9 of FIG. 5) with the departure times having asserted CBR bits; and

de-asserting the CBR bit (513 of FIG. 4, the CBR bits can be inherently asserted or de-asserted) corresponding to the departure time that matches the current time Value.

Regarding **claim 32**, Ohgane et al discloses the method of Claim 31 (as applied in claim 32 above), wherein de-asserting the CBR bit (513 of FIG. 4, the CBR bit can be inherently asserted or de-asserted) enables the corresponding departure time to participate in determining (S9, FIG. 5) which departure time is the earliest (S9-S12, FIG. 5).

Regarding **claim 33**, Ohgane et al discloses a method of scheduling packets of traffic flows having either an UBR or a CBR, comprising:

calculating a departure time (34 of FIG. 2) for each packet received;

storing the departure times for the UBR packets and for the CBR packets in a CAM device (511 of FIG. 4);

comparing the departure times (511-516 of FIG. 4) for the UBR packets with each other to determine which departure time is the earliest (S9-S12, FIG. 5); and

transmitting the packet corresponding to the earliest departure time (S13, FIG. 5).

Regarding **claim 34**, Ohgane et al discloses the method of Claim 33, further comprising:

comparing a current time value with the departure times for the CBR packets (S9 of FIG. 5).

Regarding **claim 35**, Ohgane et al discloses a method of scheduling packets of traffic flows having either an UBR or a CBR, comprising:

calculating (Line 22-30, Col. 7) a departure time (transmission time, Line 26, Col. 7) for each UBR packet;

calculating (Line 22-30, Col. 7) a departure time window (transmission time, Line 26, Col. 7) for each CBR packet;

queuing the CBR packets and the UBR packets together in the same queuing mechanism (511 and 513 of FIG. 4); and

selecting the packets for departure according to which has the earliest departure time (516 of FIG. 4).

Regarding **claim 36**, Ohgane et al discloses the method of Claim 35, further comprising:

comparing (S9 of FIG. 5) a current time (COUNTER, S9 of FIG. 5) value with the departure time (CAM WRITTEN VALUE, S9 of FIG. 5) for the CBR packets; and

selectively enabling (516 of FIG. 4) the CBR packets to participate in determining which packet has the earliest departure time in to the comparing (FIG. 5).

Claim Rejections – 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

> 1. Determining the scope and contents of the prior art.
> 2. Ascertaining the differences between the prior art and the claims at issue.
> 3. Resolving the level of ordinary skill in the pertinent art.
> 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claim 4, 10-11** and **13-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohgane et al, US Patent Number 5,875,173.

Regarding **claim 4**, Ohgane et al discloses the traffic management processor of Claim 3 (as applied in claim 3 above); but fails to disclose that only the departure times ("Transmission Time" in 511 of FIG. 4) for packets having a de-asserted CBR bit (513 in FIG. 4) participate in determining which departure time is the earliest.

However, the compare logic (40 and 51 of FIG. 3) can be easily configured to process packets only with CBR bit on (or off). It is a common practice in the art to provide simple, independent functions, then combine them to serve for different kinds of purposes, and this examiner takes Office Notice of this notion. The advantages of this

are great flexibility in selections, also the saving of resources, for example, processing power.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to configure the compare logic to process only UBR packets because of benefits of great flexibility in selections, also the saving of resources, for example, processing power.

Regarding **claim 11**, Ohgane et al discloses the traffic management processor of Claim 10 (as applied in claim 10 above), but fails to disclose wherein the departure times corresponding to packets of the CBR traffic flow are not provided to the compare logic.

However, the component that generate the departure times (34 in FIG. 3) can easily be configured to selectively provide the departure times in response to the CBR bits (the CBR bit can either be on or off). It is a common practice in the art to provide simple, independent functions (such as providing departure times only when CBR bit of the cell is on or off), then combine them to serve for different purposes, and this examiner takes Office Notice of this notion. The advantage of this is the benefit of great flexibility..

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to configure the compare logic to selectively provide the departure times in response to the CBR bits because of benefits of great flexibility.

Regarding **claim 13**, Ohgane et al discloses the traffic management processor of Claim 12 (as applied in claim 12 above), but fails to disclose wherein the CAM device is

configured to compare the current time value to only those departure times having an asserted CBR bit.

However, the compare logic (41 and 51 in FIG. 3) can easily be configured to selectively compare the current departure times value to only those departure times having an asserted CBR bit. It is a common practice in the art to provide simple, independent functions (such as comparing the current time value to only those departure times having an asserted or de-asserted CBR bit), then combine them to serve for different purposes, and this examiner takes Office Notice of this notion. The advantage of this is the benefit of great flexibility..

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to configure the compare logic to compare the current departure times value to only those departure times having an asserted CBR bit, because of benefits of great flexibility.

Regarding **claim 14 and 15**, Ohgane et al discloses the traffic management processor of Claim 13 (as applied in claim 13 above), but fails to disclose wherein the CAM device is configured to selectively de-assert the CBR bits in response to match conditions in the CAM device, and de-assertion of the CBR bit enables the corresponding departure time to participate in determining which departure time is the earliest.

The purpose of de-assertion of CBR bit is to produce the corresponding departure time for each CBR packet so that it can be use by the compare logic. Ohgane et al discloses that the departure time of each CBR packet is generated by 34 of FIG. 2,

using different traffic parameters (Line 20-25, Col. 6), and then is put in a queue (511 of FIG. 4) for the compare logic to process (FIG 4). In this way the same functionality of claims 14 and 15 is achieved.

The disclosure by Ohgane et al calculates the departure times for both CBR and ABR packets with the same mechanism (22-30, Col 7), only the parameters used are different. Using the same mechanism to implement different functionalities with different parameters is a common practice in the art that reduces the manufacturing and/or design complexity and cost of the implementation.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to calculate the departure times with the mechanism disclosed by Ohgane et al because of the great benefits of reducing manufacturing and/or design complexity and cost.

Response to Arguments/Remarks

5. **Applicant's** arguments filed on 4/2/2007 have been fully considered but they are not persuasive.

According to MPEP claims should be given "the broadest reasonable interpretation" (Bullet 2 of H Subsection in MPEP 708(a)), and prior art should "particular emphasis on the **inventive concept** towards which the claims are directed" (PCT Rule 33.3(a), see MPEP 1843.01). Therefore, Examiner interprets a claim in a broadest reasonable way and focuses on inventive concept the claim.

6. For **remarks** on Independent claim1, which are also applied to Claims 2-15 (8th line from the bottom of Page 10 to Line 8 of Page 12), Applicants argue that "Ohgane

fails to disclose or suggest a traffic management processor of Applicants' Claim 1" because "collating register 513 is NOT part of the CAM 511" (Line 14 of Page 11) and

In response, Examiner disagrees.

First, a CAM is referred to as a hardware device with a combination of logic and memory that is capable of searching and processing each row (or item which is a packet/cell/frame in this case) in a table (in CAM memory) quickly without the intervention of CPU. CAM is widely used in the industry as shown by Ohgane. There is nothing novel in using a CAM device to process packets;

Secondly, the device shown by Ohgane (FIG. 1) is conceptually identical to the CAM device recited by the application as explained in details in this Office Action above; specifically, the Office Action interprets a row of the table as all the information related to a packet; searching and processing are done based a unique key (which can be flow ID or Departure time or the combination of several independent parameters) of the row; Ohgane clearly discloses such a CAM device since each row of it include all the information of the row of application, including departure time and the bit that can be used to determine whether the packet is belong to specific traffic type such as CBR. Notice that interpretation of the row does not limit all pieces of row information being physically located in a same device such as 511 of FIG. 4 in Ohgane, some pieces of row information may locate in other parts of the CAM device such as 513 of FIG. 4 and 27 of FIG. 1.

7. For remarks on Independent Claim16, which are also applied to claim 16-21 (Line 9 of Page 12 to Line 10 of Page 14), Applicants argue that "Ohgane fails to

disclose or suggest a traffic management processor of Applicants' Claim 16" because the CAM device that Ohgane discloses is for RM cell (Line 2-3 of Page 13).

In response, Examiner disagrees because the inventive conception of Ohgane's CAM device can applied to normal cell as well, due to the fact that ATM RM cell header is same as the normal ATM cell header.

8. For remarks on Independent Claim 22, which are also applied to Claims 23-27 (Line 11 of Page 14 to 4th line from the bottom in Page 15), Applicants argue that "Ohgane fails to disclose or suggest a traffic management processor of Applicants' Claim 22" because of the following reasons:

a) the departure time window is not disclosed by Ohgane (Line 4-5 of Page 15);

b) "queuing the CBR packets and the UBR packet together" is not disclosed by Ohgane (Lines 10-11 of Page 15).

In response, Examiner disagrees with the reasons explained as follows:

a) according to the specification the departure time for a CBR packet is the current time plus departure time window ([0007]), whose calculation is well known in the art; therefore, the departure time by Ohgane inherently includes the departure time window of the application (the departure time for a UBR packet is not related to departure time window according to Specification [0007]);

b) arranging packets according to their departure time is a special kind of queuing, and the queuing include both CBR and UBR packets and the departure time for both of them are placed in the same table/array; therefore, Ohgane does disclose "queuing the CBR packets and the UBR packet together".

9. For remarks on Independent Claim 28, which are also applied to Claims 29-32 (from Line 3 from the bottom of Page 15 to Line 2 of Page 17), Applicants argue that "Ohgane fails to disclose or suggest a traffic management processor of Applicants' Claim 28" because of the following reasons:

a) "queuing the CBR packets and the UBR packet together" is not disclosed by Ohgane, this is the same reasoning as that of b) for Claim 22;

b) collating register 513 is NOT part of the CAM 511, this is the same reasoning as that of Claim 1;

In response, Examiner disagrees with the reasons explained as follows:

a) the explanation presented above for b) of Claim 22 is applied;

b) the explanation presented above for Claim 1 is applied.

10. For remarks on Independent Claim 33, which are also applied to claim 34 (from Line 3 of Page 17 to Line 19 of Page 18), Applicants argue that "Ohgane fails to disclose or suggest a traffic management processor of Applicants' Claim 33" because of the following reasons:

a) the same reasoning as that of b) for Claim 22;

b) "transmission time is ***not compared with each other***" in Ohgane;

In response, Examiner disagrees with the reasons explained as follows:

a) the explanation presented above for b) of Claim 22 is applied;

b) The comparison of transmission time of packets (including both CBR and UBR) to each other is done by SELECTOR (516 of FIG. 4) as clearly shown in FIG. 4 of Ohgane.

11. For remarks on Independent Claim 35, which are also applied to claim 36 (from Line 20 of Page 18 to Line 22 of Page 19), Applicants argue that "Ohgane fails to disclose or suggest a traffic management processor of Applicants' Claim 35" because of the following reasons:

a) the same reasoning as that of a) for Claim 22;

b) the same reasoning as that of b) for Claim 22;

In response, Examiner disagrees with the reasons explained as follows:

a) the explanation presented above for a) of Claim 22 is applied;

b) the explanation presented above for b) of Claim 22 is applied.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jianye Wu whose telephone number is (571)270-1665. The examiner can normally be reached on Monday to Friday, 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on (571)272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jianye Wu

Lana Le
5-09-07
LANA LE
PRIMARY EXAMINER